deposition capability of the material for forming at least one component (at least either the first signal electrode or ferroelectric layer) of the ferroelectric capacitors to be formed in the succeeding steps. As shown in Fig. 25, as ~~As~~ a modification example, the undercoat layers 22 may be formed in the first regions 24. The ferroelectric capacitors may be selectively formed in the first regions 24 by preparing the material for forming at least one component of the ferroelectric capacitors so as to have a composition in a liquid phase or a vapor phase so that the material is deposited preferentially on the surface of the undercoat layers 22.

Please replace the Abstract filed with the attached amended Abstract. Following is a marked-up version of the amended Abstract:

ABSTRACT OF THE DISCLOSURE

The present invention relates to: a memory cell array which is capable of decreasing the ~~parasitic capacitance~~ parasitic capacitance or load capacitance of signal electrodes and has ferroelectric layers making up ferroelectric capacitors and having a predetermined pattern; a method of fabricating the memory cell array, and a ferroelectric memory device. In the memory cell array, memory cells formed of ferroelectric capacitors are arranged in a matrix. The ferroelectric capacitors include first signal electrodes, second signal electrodes arranged in a direction intersecting the first signal electrodes, and ferroelectric layers disposed linearly along either the first signal electrodes or the second signal electrodes. Alternatively, the ferroelectric layers may be disposed only in intersection areas of the first and second signal electrodes.